



Transcede™



➤ Solving 4G Challenges for Pico,
Micro and Macrocell Platforms

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CTO

Communications Convergence Processing
Mindspeed Technologies, Inc.

MINDSPEED
BUILD IT FIRST®

August 24, 2010

The Next Internet Wave – Mobility and Content

Innovative New Platforms



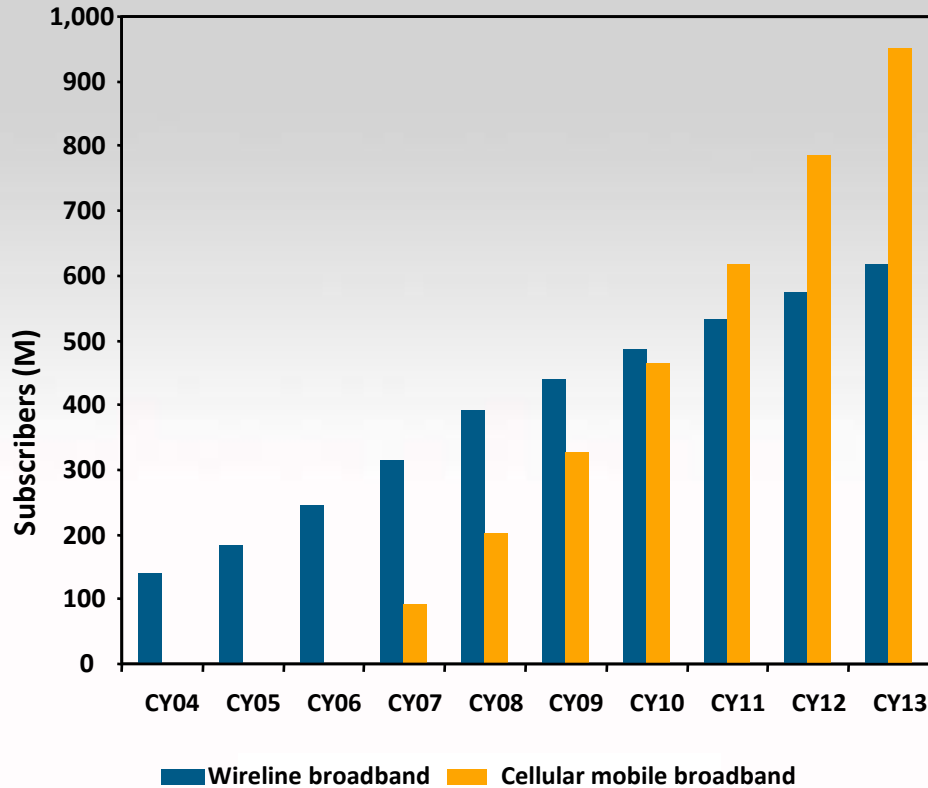
+

New Networked Applications

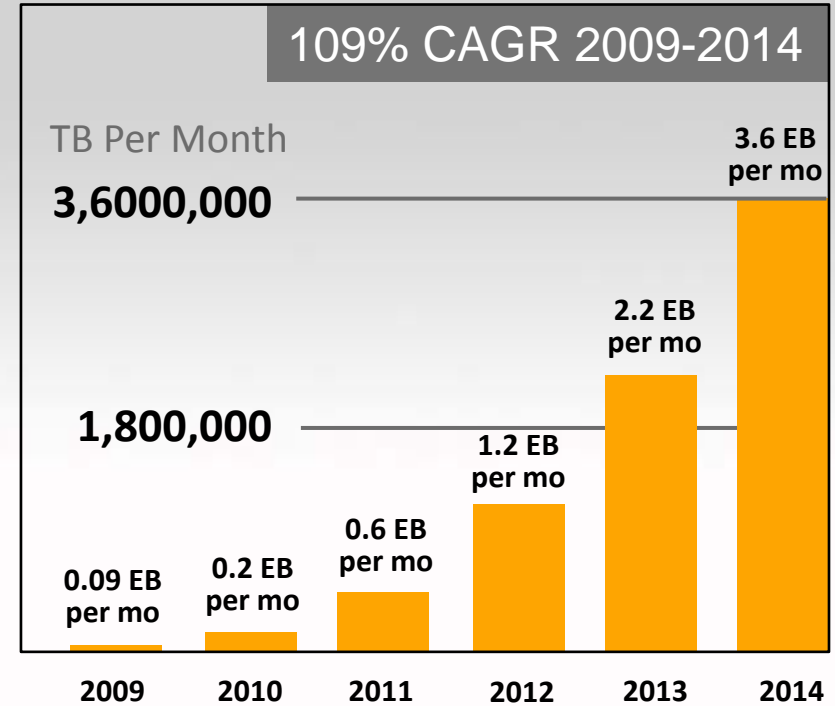


= Explosive demand for Mobile Broadband

Impact on Service Providers



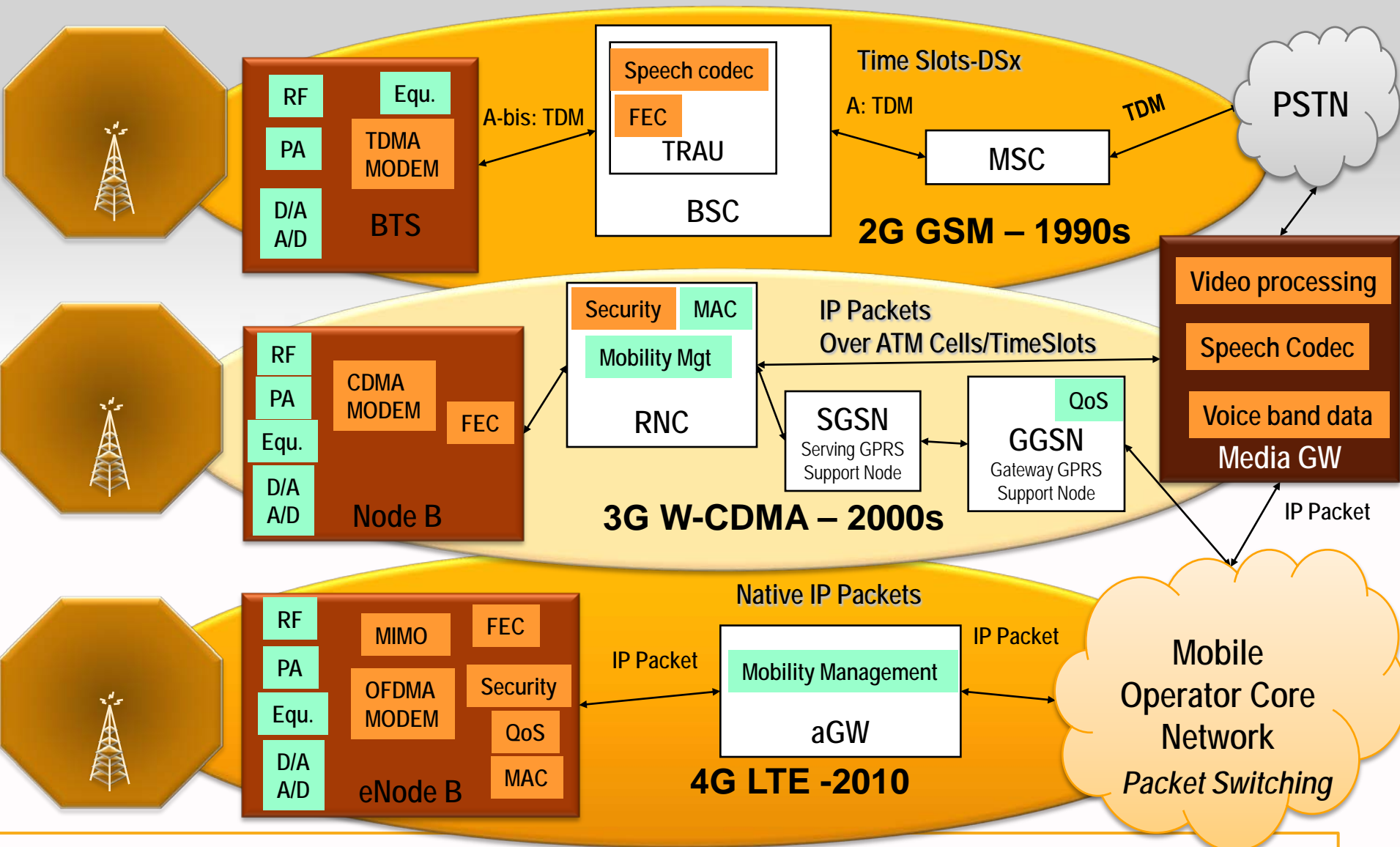
Source: Infonetics Q4'2009



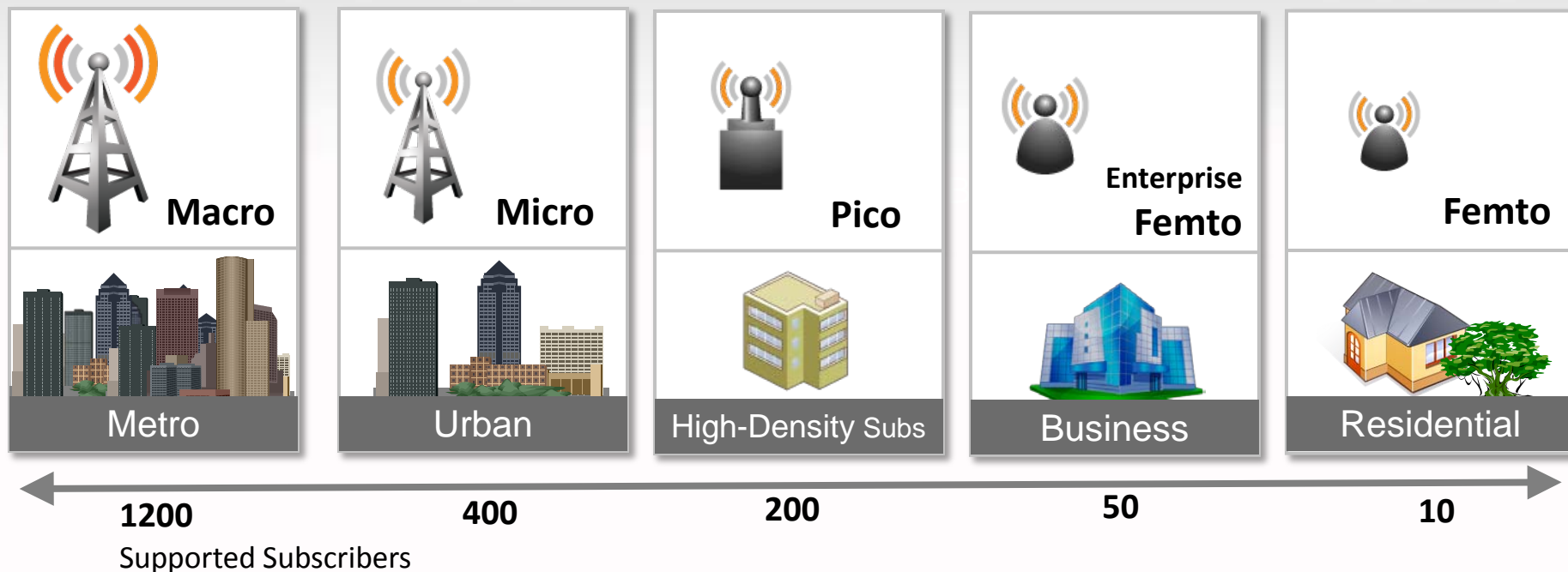
Source: 2010 Cisco VNI Mobile

... Overloaded Networks

2G to 4G - System Architecture Evolution - to the Evolved Packet Core



Mobile Broadband Architecture – Going Distributed

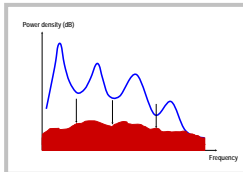


Serving a broad range of basestations - from Macro to Femto

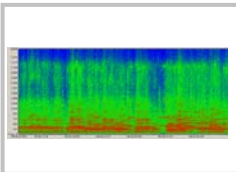
Mindspeed SoC Competencies



Multi-Processor Communications Technologies



Algorithms



Standards
Certification

Multi-Core Software

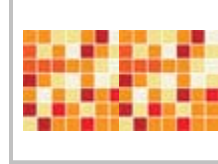


Software
Verification



Software
Architecture

Convergence Applications



Packet
Processing

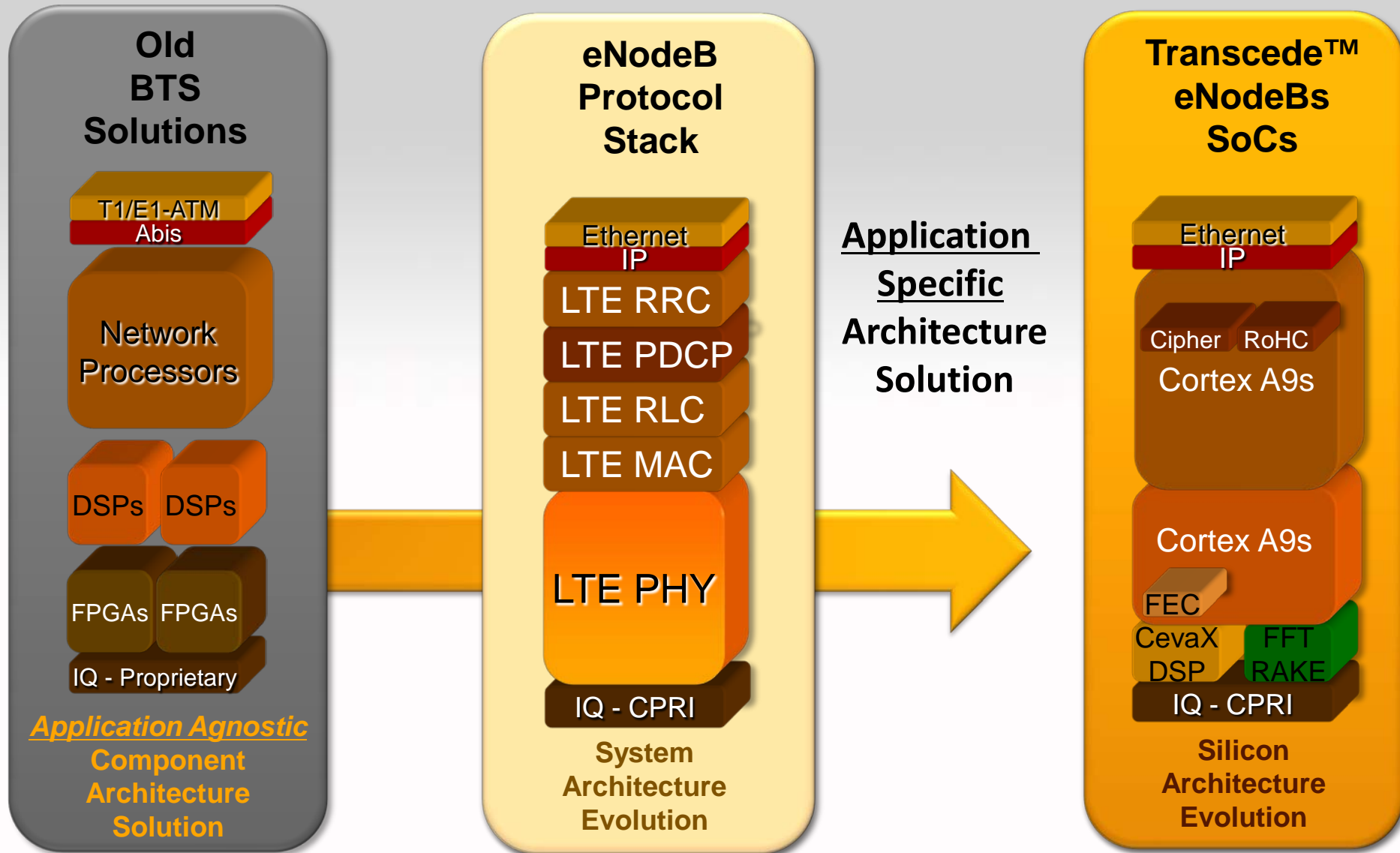


Voice, Video,
and Modems

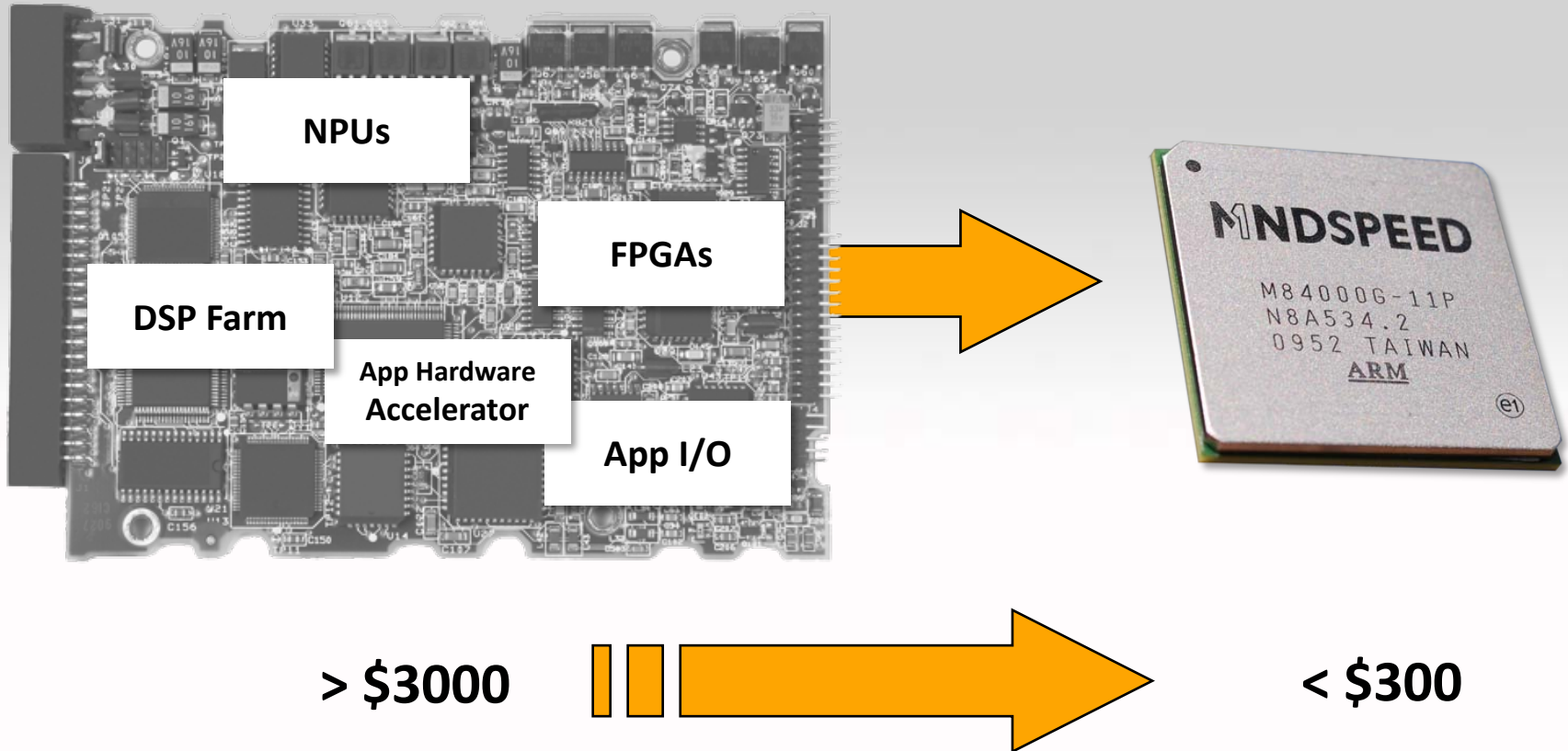


Silicon Architecture Evolution

Silicon & System Architecture Innovation

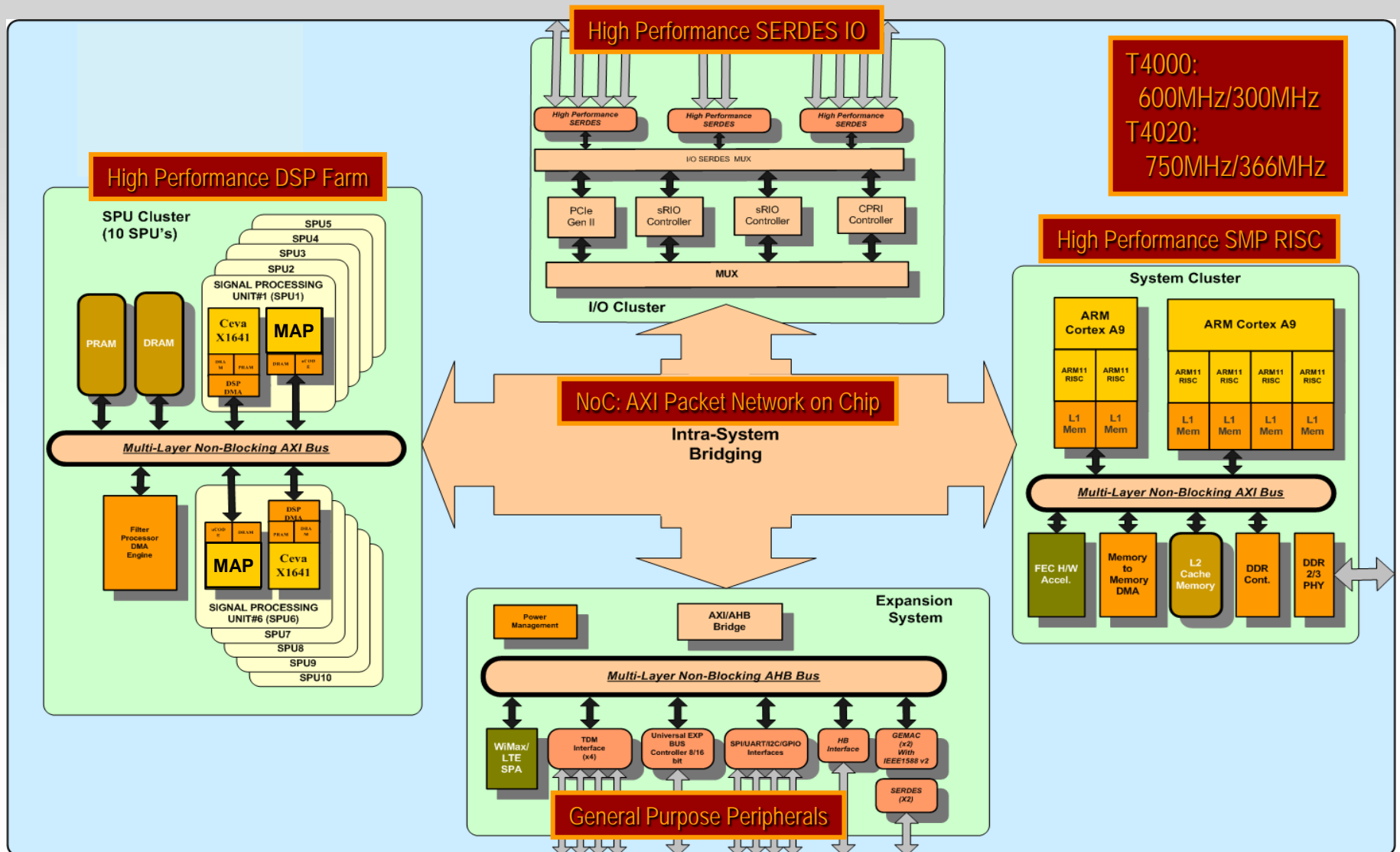


Transcede™ Dramatically Reduces System BOM



... while significantly accelerating Time-to-Market

eNB Transcede™ - Multi-Core SoC



Processors: Instruction and Data Level Parallelism



High Efficiency
Instruction Level
Parallelism



High Efficiency
Instruction & Data Level
Parallelism

MINDSPEED®

MAP

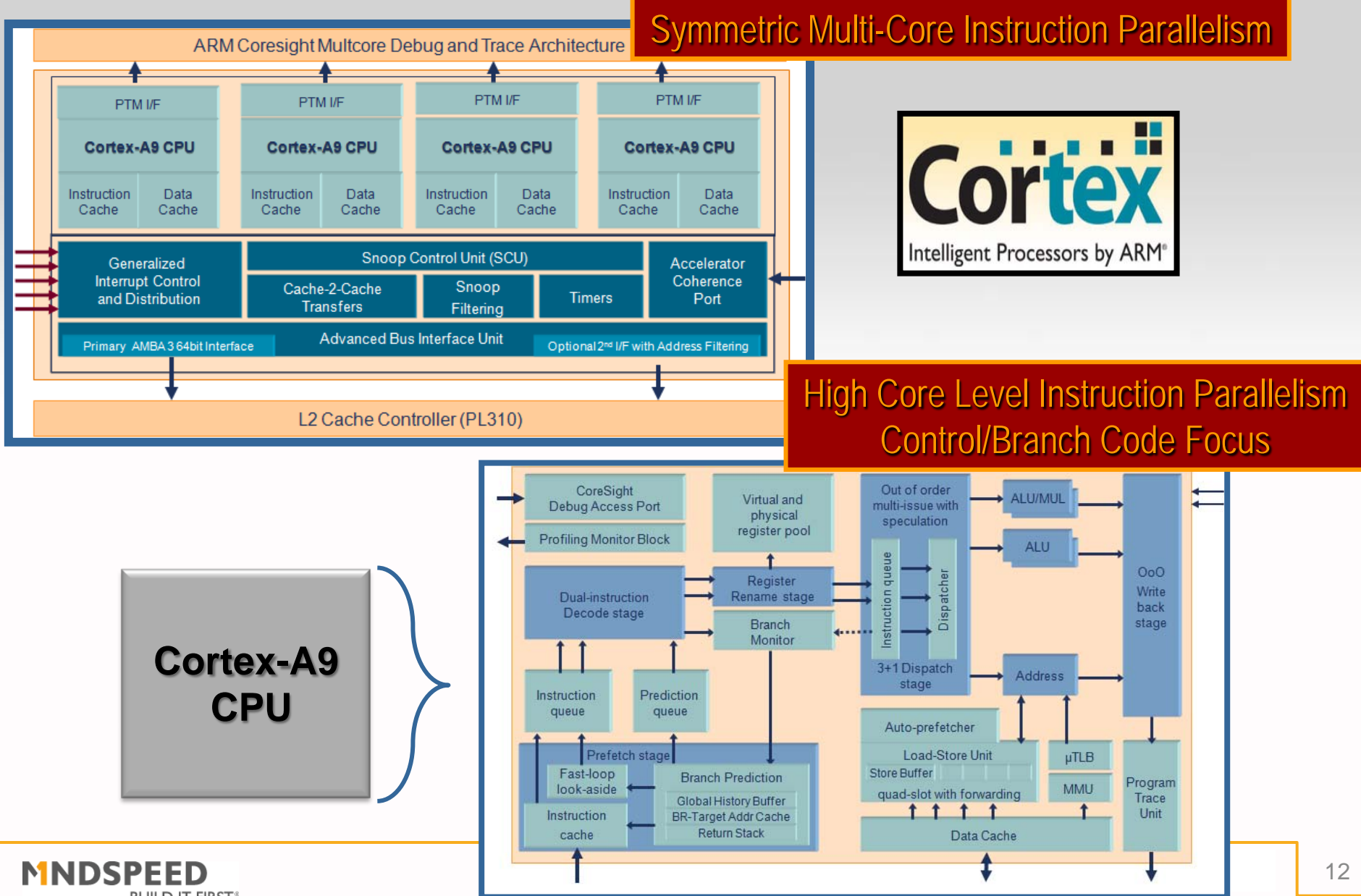
High Efficiency Data Level Parallelism

- **600MHz to 750MHz Operation**
- **4 A9 Multi-Processing Cores**
 - SMP & AMP support
 - Parallel Cores with HW Snoop Logic
 - 32bit Instructions
 - Load/Store Register File
 - 13 stage Pipeline
- **Small L1 Memories**
 - 32kB Program Cache
 - 32kB Data Cache
- **Large L2 Memories**
 - **512kB Unified Cache**
- **Embedded Trace Module**
 - Complex Instruction Diagnostics
- **Dual Data/Program DMA/Cache**
- **Extensive Tool Chain**
 - C-Compilers/Debugger/etc.

- **600MHz to 750MHz Operation**
- **256bit-8 Way VLIW DSP**
 - 8-32bit Parallel Instructions
 - Most common size
 - 16-16bit Parallel Instruction
 - 9 stage Pipeline
- **128bit 4/8 MAC SIMD**
 - 4- 16bit x 16bit MACs
 - 8- 8bit x 8bit MACs
- **Large L1 Memories**
 - 96kB Program RAM
 - Direct Mapped Cache Option
 - 128kB Data RAM
 - Banked Simultaneous Access
- **On-chip Emulation Module**
 - Complex Breakpoints/Trace/etc.
- **Dual Data/Program DMA/Cache**
- **Extensive Tool Chain**
 - C-Compilers/Debugger/etc.

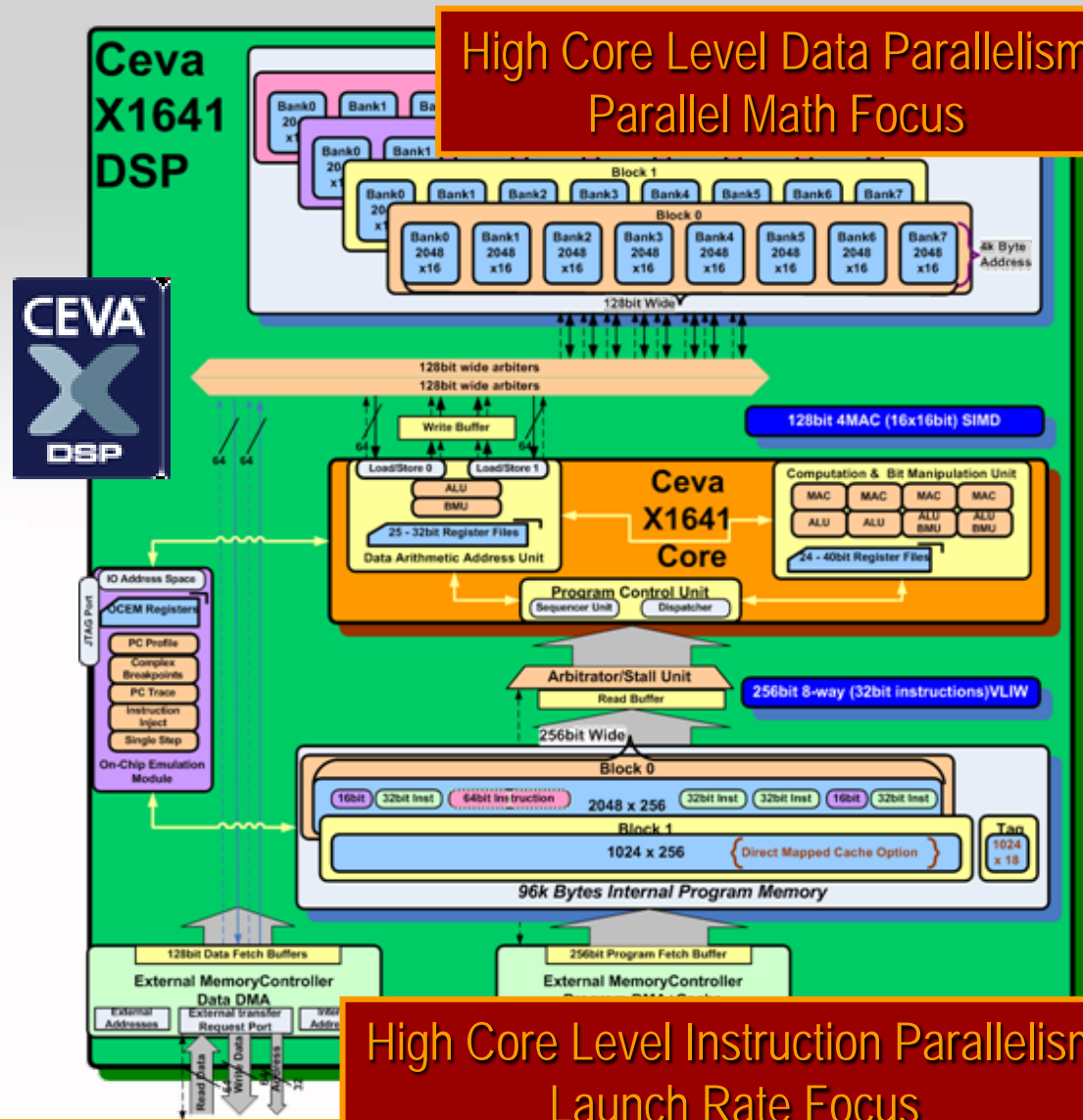
- **600MHz to 750MHz Operation**
- **160bit-VLIW DSP**
 - Fine Grain VLIW
- **160bit SIMD**
 - 24bit x 16bit MACs
- **Built in FFT Radix Support**
- **Large L1 Memories**
 - 10kB Program RAM
 - 80kB Data RAM
 - Banked Simultaneous Access
- **External Sequencer Control**
- **High Performance DMA**
- **Side-band Multi-Core Sequencing Control Channel**
 - **Processor to Processor Pipelined Data Flow**

Processors: Instruction and Data Level Parallelism



600MHz to 750MHz CevaX1641 8-way VLIW DSP

- **600MHz to 750MHz Operation**
- **256bit-8 Way VLIW DSP**
 - 8-32bit Parallel Instructions
 - Most common size
 - 16-16bit Parallel Instructions
- **128bit 4/8 MAC SIMD**
 - 4- 16bit x 16bit MACs
 - 8- 8bit x 8bit MACs
- **Large L1 Memories**
 - 96kB Program RAM
 - Direct Mapped Cache Option
 - 128kB Data RAM
 - Banked Simultaneous Access
- **On-chip Emulation Module**
 - Complex Breakpoints/Trace/etc.
- **Dual Data/Program DMA/Cache**
- **Extensive Tool Chain**
 - C-Compilers/Debugger/etc.

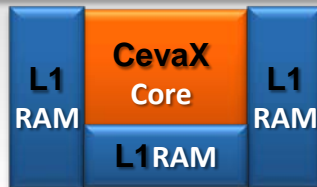


Mindspeed Application Processor

Programmable Application Specific Signal Processing

General Purpose Signal Processor

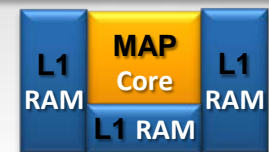
62.5% RAM, 37.5% Core



Simplified Instruction Pipeline
Limited Control Code Focus
Small PRAM, L1 sized to limited function focus

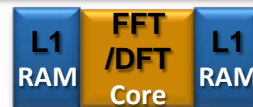
Application Specific Signal Processor

45% RAM, 55% Core



Fixed Function Signal Processing

35-40% RAM, 60-65% Core

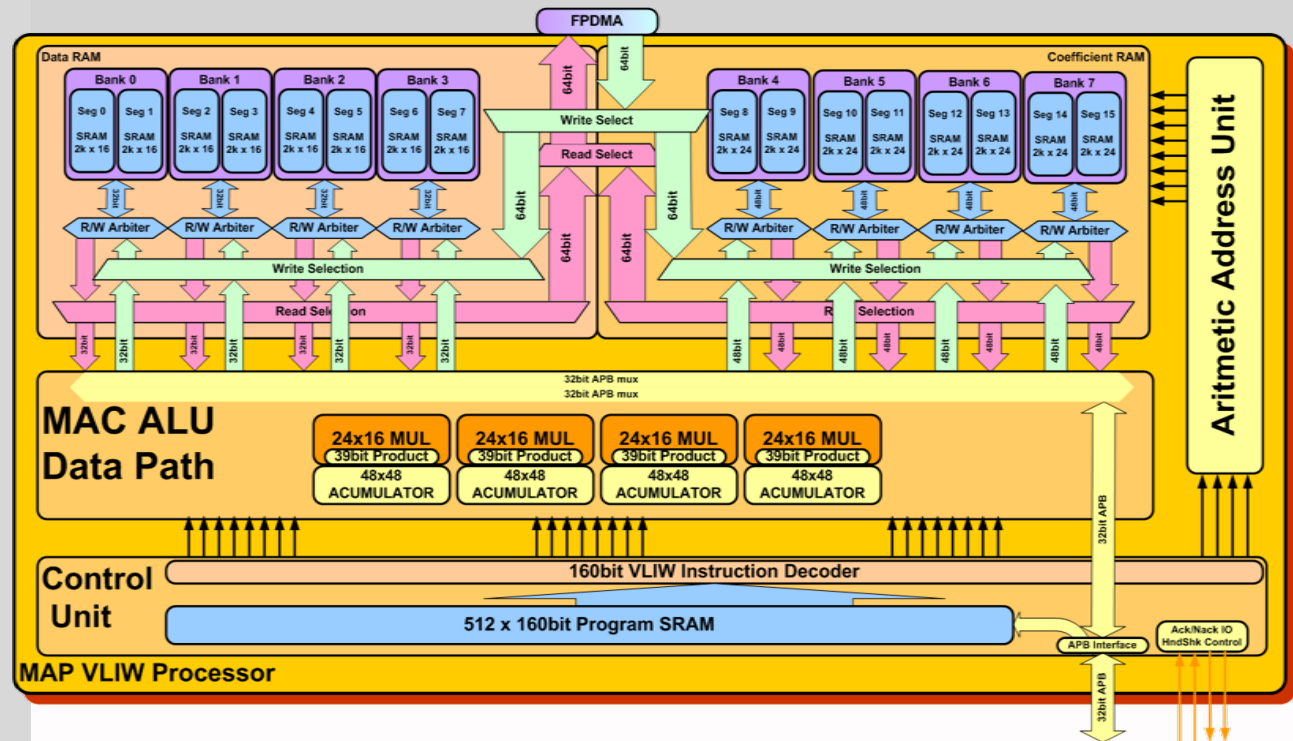


No Instructions
State Machine Control
RAM sized to one function

Limited Savings For Loss
In Application Flexibility

Mindspeed Application Processor (MAP)

- 600MHz to 750MHz Operation
- 160bit-1 Way VLIW DSP
- 160bit 4 MAC SIMD
 - 4- 24bit x 16bit MACs
- Built in FFT Radix Support
 - Bit Reverse Addressing
- Circular Buffering
- Built in Byte Data RAM read
- Very Wide/Large L1 Memories
 - 10kB Program RAM,
 - 80kB Data RAM
 - Banked Simultaneous Access
- External Sequencer Control
- High Performance DMA for Data
- 4G/3G Application Library

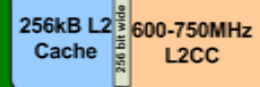
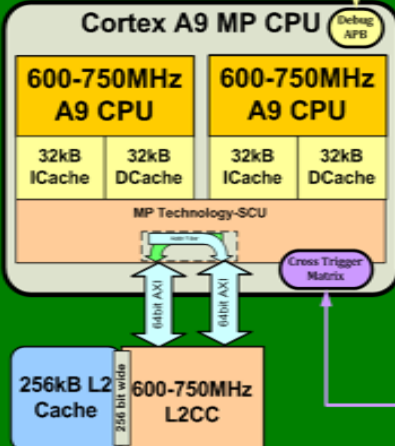
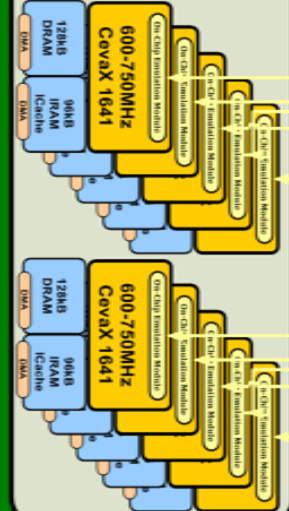


CoreSight™ SoC HW SW Debug Support

RealView®
Tools by ARM®

**3G WCDMA HSPA+ &
4G OFDMA LTE PHY**

**CevaX1641
DSP Farm**

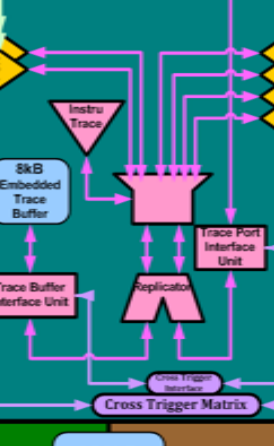


CoreSight Debug HW

JTAG Port External Trace Port

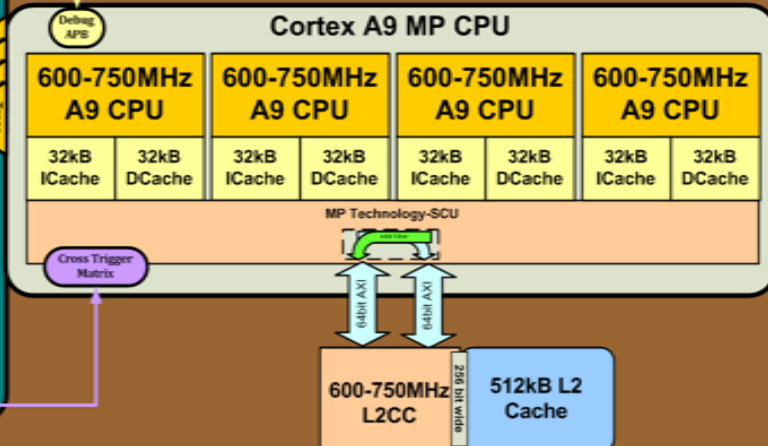
Debug Access Port

System Time Stamp Counter



**Tightly coupled MAC/PHY
Streaming Real-Time Debug Capability!**

Cortex®
Intelligent Processors by ARM®



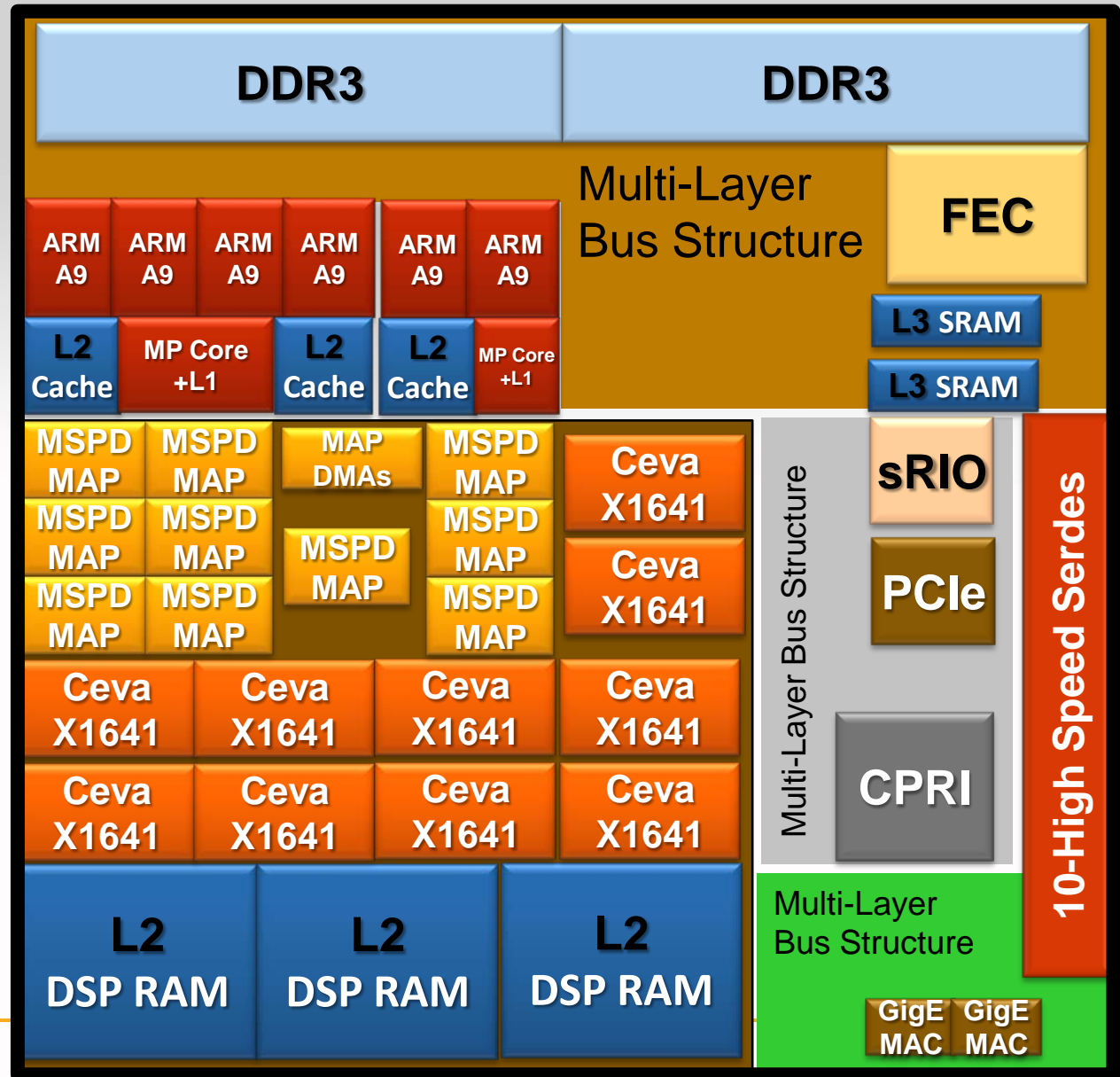
3G/4G MAC



Transcede™ 4000 SoC



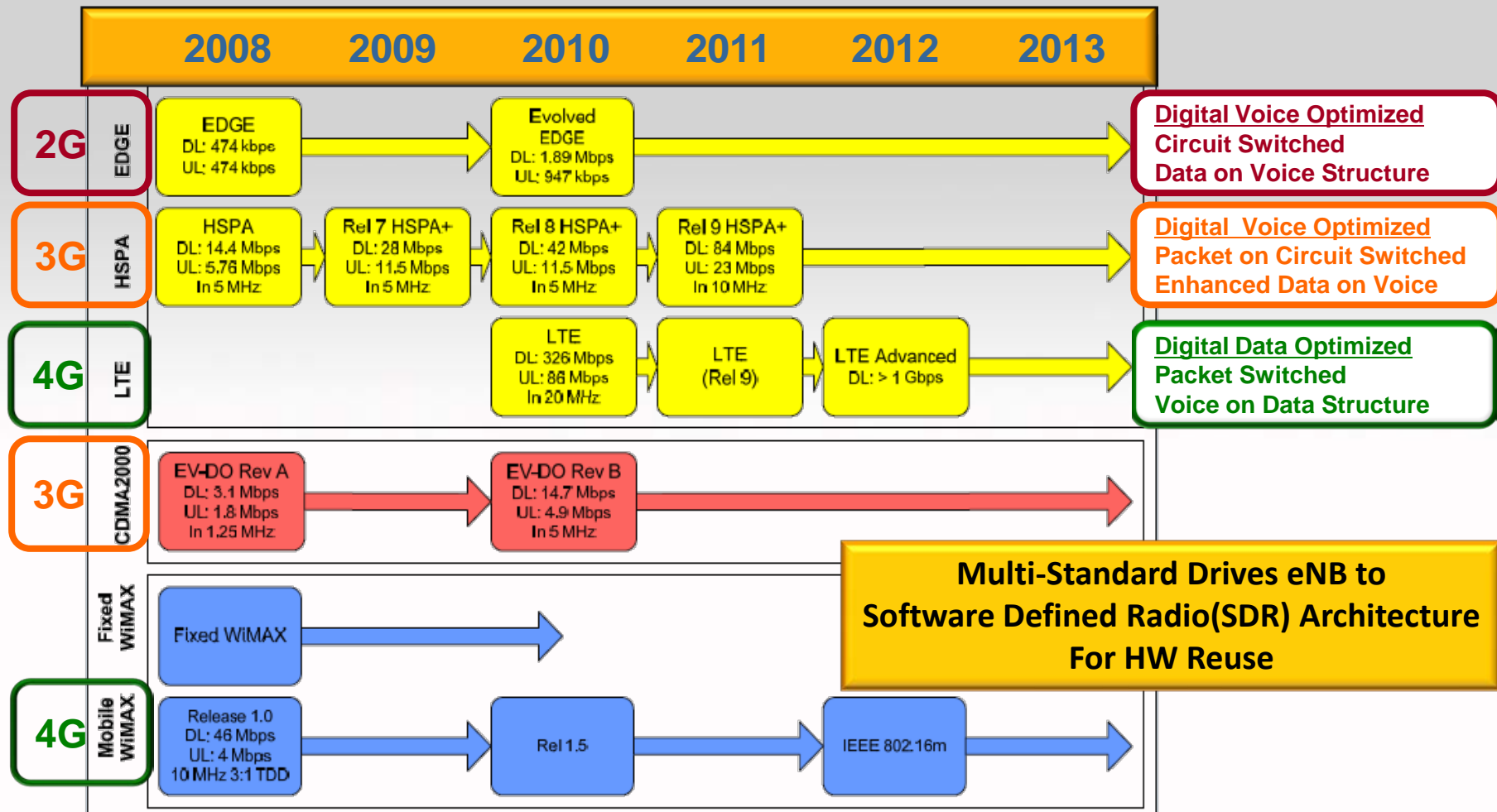
- TSMC 40G Process 0.9V
- 12W typical
- 31mm x 31mm
- 26 Processors
- 9.1MBytes RAM
- >300M transistors





Software Architecture Evolution

Mobile Data Link Standards Evolution

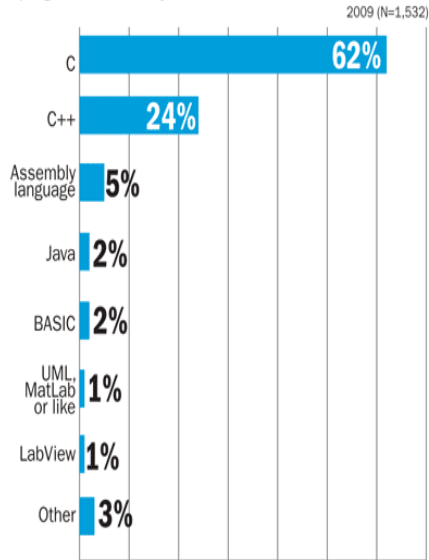


Notes: Throughput rates are peak theoretical network rates. Radio channel bandwidths indicated.
 Dates refer to expected initial commercial network deployment except 2008, which shows available technologies that year.

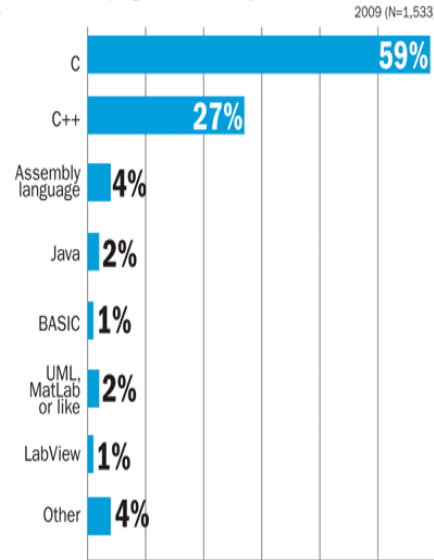
Innovation in Multi-Core Programming

C language dominates today's and tomorrow's sequential programs

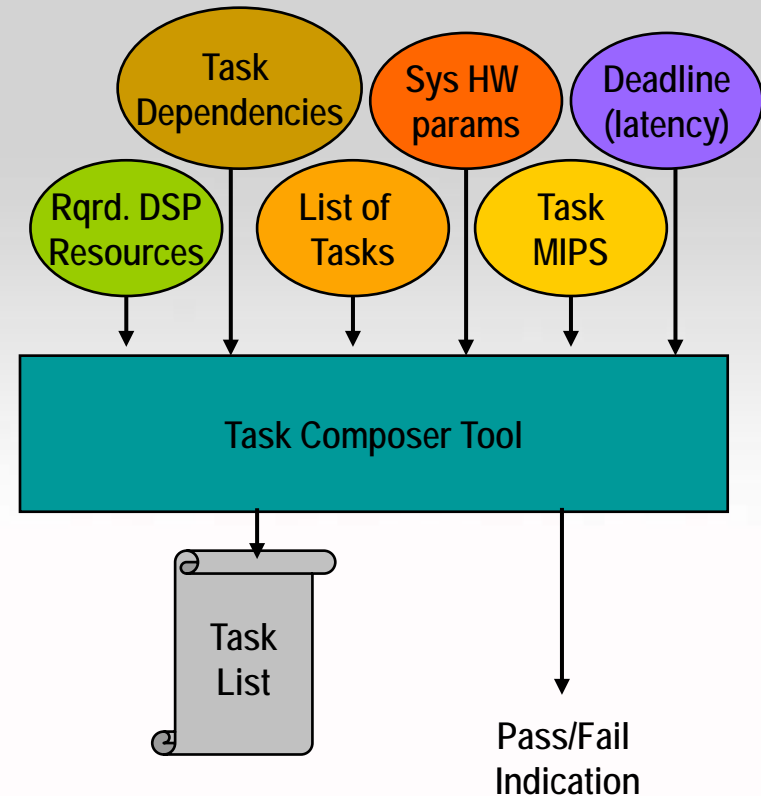
My **CURRENT** embedded project is programmed mostly in:



My **NEXT** embedded project will likely be programmed mostly in:



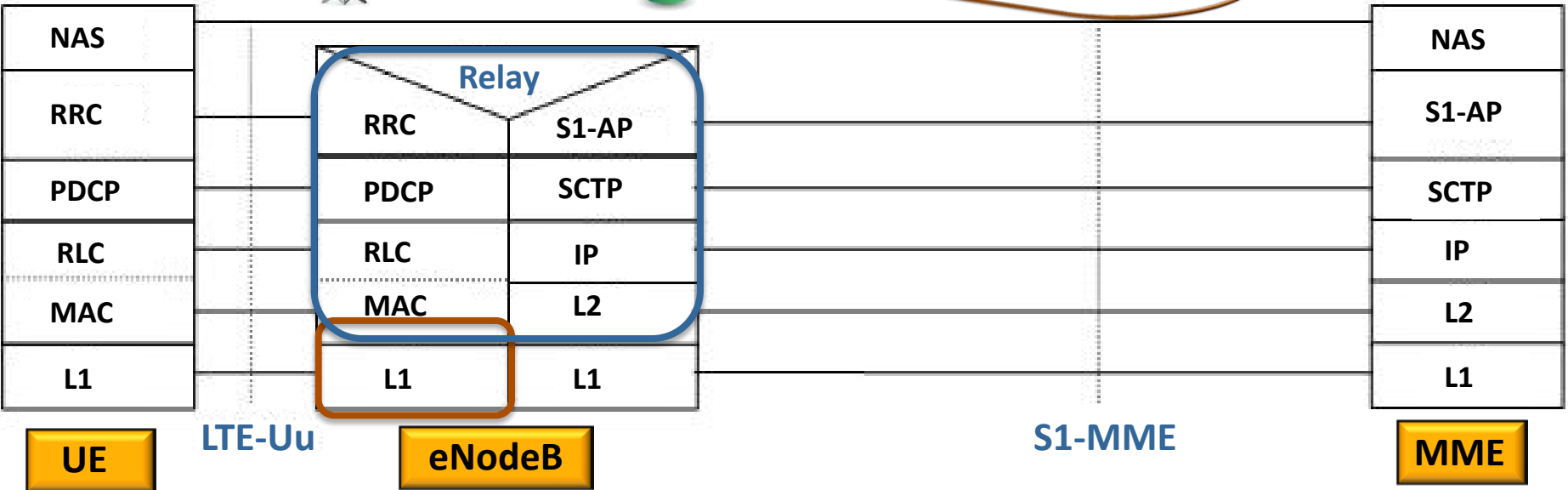
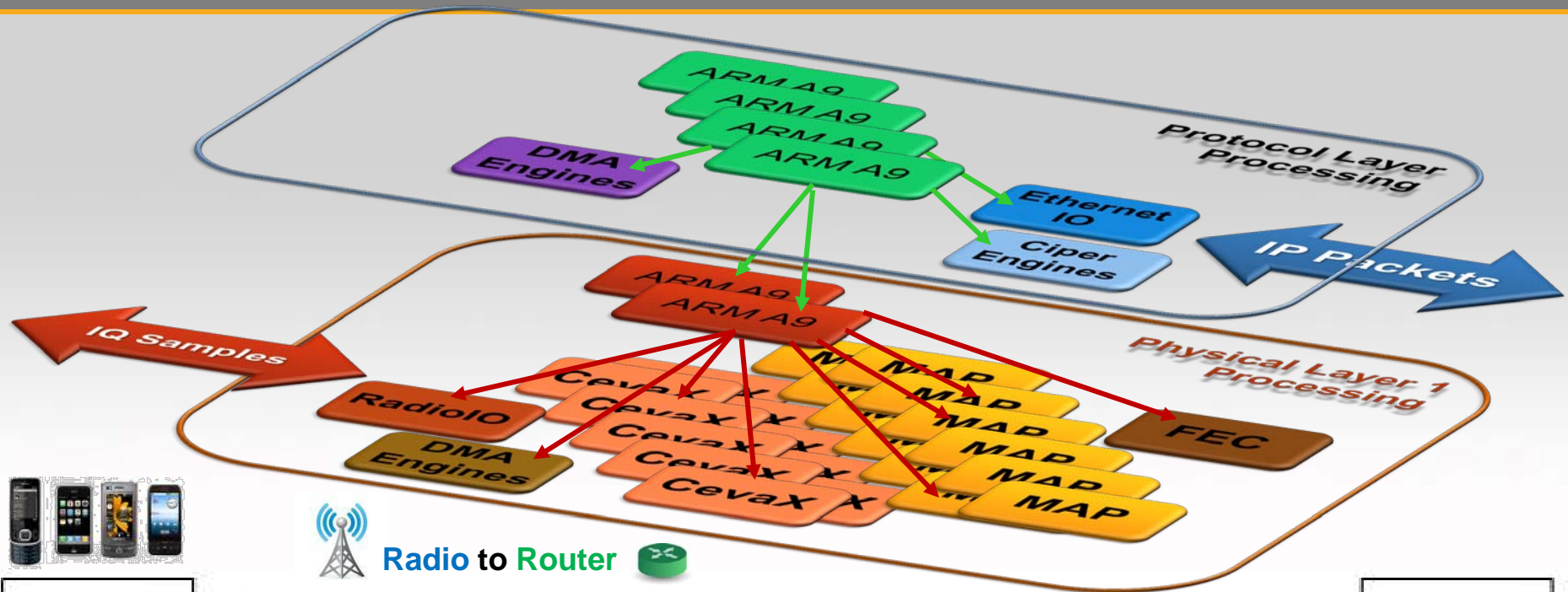
SOURCE: TechInsights' 2009 Embedded Market Study



However, C is a sequential language, so how do application developers map their C code into multi-core SoCs?

New modeling approach allows application partitioning and profiling early on in the design phase

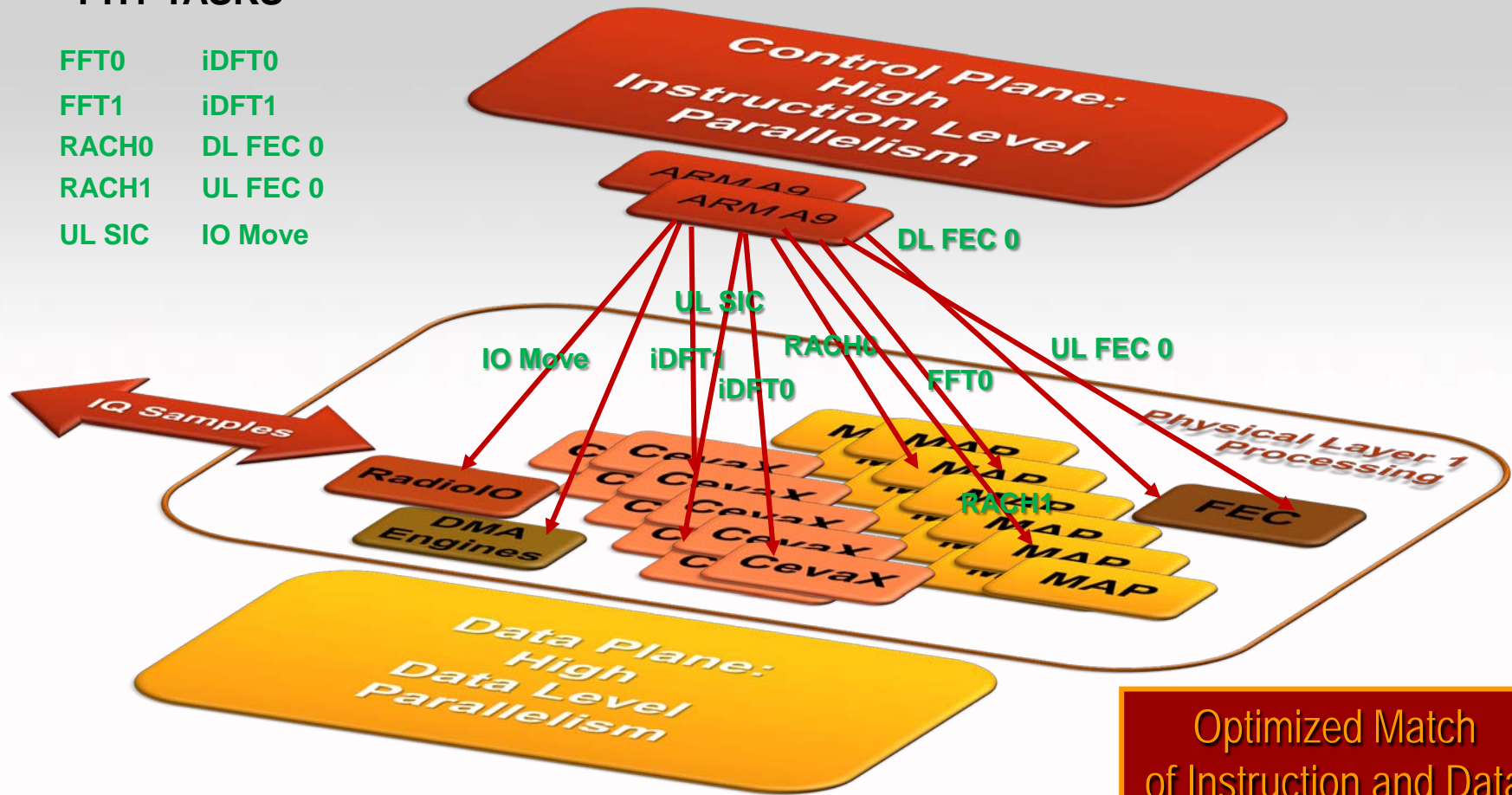
Software Multi-Core HW Mapping: LTE PHY & L2



Software Multi-Core HW Mapping: LTE PHY

PHY TASKS

FFT0	iDFT0
FFT1	iDFT1
RACH0	DL FEC 0
RACH1	UL FEC 0
UL SIC	IO Move



Optimized Match
of Instruction and Data
Parallelism

Key Differentiators of the Transcede™ Family

- Software configurable for all flavors of LTE, W-CDMA and WiMAX (SDR)
 - Supports China standards, including TD-SCDMA and TD-LTE
- Significantly reduces system bill of materials
- Integrated L2 and L1 on a single SoC provides lowest possible latency
- Simplified programming model allows easy adaptation
- Roadmap of scalable SoCs delivers a range of performance/cost points across the range of base stations

**THANK
YOU!**

